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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,704	12/21/2001	Mauricio Calle	9-5-9-4-1	3882

7590 08/11/2004

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/029,704	Applicant(s) CALLE ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

1. The abstract of the disclosure is objected to because it exceeds 250 words.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "first classification circuitry configurable to determine for a given packet received by the processor whether the packet has one or more errors"

[Emphasis Added]. The recited claim language is indefinite since it is not clear that the language imparts a structural limitation, i.e., a circuit only has to be configurable to “determine for a given packet received by the processor whether the packet has one or more errors”, but does not have to perform the actual error detection (Note: any processor is configurable to detect errors through the use of software even if it is not currently running any software).

Claim 1 recites, “the scheduling circuitry **being configurable** based on the indication of the error determination to control the performance of at least one of: (i) dropping of the given packet, and (ii) directing the given packet to the second classification circuitry” [Emphasis Added].

Claim 1 recites, “**adapted to** receive an indication” [Emphasis Added]. The recited claim language is indefinite since it is not clear that the language imparts a structural limitation, i.e., a circuit only has to be adapted to “receive an indication”, but does not have to actually receive an indication (Note: any receiver is adapted to “receive an indication” even if it never receives an indication since a receiver can receive data signals).

Claim 2 recites, “**configurable** based on the indication of the error determination to control the dropping of the packet if the packet has one or more errors” [Emphasis Added].

Claim 3 recites, “**configurable** based on the indication of the error determination to direct the given packet to the second classification circuitry” [Emphasis Added].

Claim 3 recites, “**configurable** to perform at least one classification operation for the given packet” [Emphasis Added].

Claim 4 recites, “**configured** to provide an interface for communication of the packet between a network and a switch fabric” [Emphasis Added].

Claim 6 recites, “**configured** to perform at least a portion of at least one of a reassembly operation” [Emphasis Added].

Claim 7 recites, “**configured** to generate a transmit command specifying a destination identifier for the given packet” [Emphasis Added].

Claim 17 recites, “**configured** as an integrated circuit” [Emphasis Added]. In addition, it is not clear whether a processor configured as an integrated circuit is an integrated circuit or not.

Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 1 recites, “second classification circuitry coupled to the scheduling circuitry”. The omitted structural cooperative relationships are: the relationship between “second classification circuitry” and “the scheduling circuitry”. Note: it is unclear how the “second classification circuitry” relates to the rest of the circuitry claimed in claim 1.

Claims 2-17 depend from claim 1, hence inherit the deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Picazo, Jr.; Jose J. et al. (US 5720032 A, hereafter referred to as Picazo).

35 U.S.C. 102(b) rejection of claims 1, 2, 17 and 18.

Picazo teaches a first classification circuitry configurable to determine for a given packet received by the processor whether the packet has one or more errors (col. 32, lines 11-16 in Picazo teach that LAN Controller Chips LCCs 110 and 180 in Figure 9 have an error correction and detection function for performing error detection; hence the error correction and detection function in LAN Controller Chips LCCs 110 and 180 are a first classification circuitry configurable to determine for a given packet received by the Hub/Bridge processing circuitry 130 whether the packet has one or more errors); scheduling circuitry coupled to the first classification circuitry and adapted to receive an indication of the error determination made by the first classification circuitry (Step 342 in Figure 5A of Picazo is a step for determining if a given packet received by the Hub/Bridge processing circuitry 130 in Figure 2 and 3 has one or more errors; Note: col. 6, lines 33-34 in Picazo teach that Figure 5A-5B is a bridge process performed by

Bridge Circuitry in Figures 2-4 in Picazo, hence Bridge Circuitry in Figures 2-4 in Picazo is scheduling circuitry coupled to the first classification circuitry and adapted to receive an indication of the error determination made by the first classification circuitry); and second classification circuitry coupled to the scheduling circuitry (Figure 5B in Picazo teach that good packets are forwarded to LAN interface and LAN interface controllers, hence LAN interface and LAN interface controllers are second classification circuitry coupled to the scheduling circuitry); the scheduling circuitry being configurable based on the indication of the error determination to control the performance of at least one of: i. dropping of the given packet, and ii. directing the given packet to the second classification circuitry (Step 342, 344 and 346 in Figure 5A of Picazo is a step for dropping of a given packet or redirecting the packet, hence scheduling circuitry Bridge Circuitry in Figures 2-4 in Picazo is configurable based on the indication of the error determination to control the performance of at least one of: i. dropping of the given packet, and ii. directing the given packet to the second classification circuitry).

35 U.S.C. 102(b) rejection of claims 3 and 19.

Col. 5, lines 9-15 in Picazo teach that after packet reception is complete and error detection has been done and the packet is deemed to be correct, the LAN controller sets another bit in the receive portion of the portion of the descriptor ring that is devoted to that LAN controller indicating that the packet has been correctly received (Note: setting another bit in the receive portion of the portion of the descriptor ring is a step for

performing at least one classification operation for the given packet if the packet is supplied thereto by the scheduling circuitry).

35 U.S.C. 102(b) rejection of claim 4.

The Abstract in Picazo teach that the processor is configured to provide an interface for communication of the packet between a network and a switch fabric.

35 U.S.C. 102(b) rejection of claim 5.

The Abstract in Picazo teach that classification operations performed by at least one of the first and second classification circuitry are programmable via software deliverable to the processor via an associated host device.

35 U.S.C. 102(b) rejection of claim 6.

See col. 42, lines 25-30 in Picazo. Note: CRC is a parity check.

35 U.S.C. 102(b) rejection of claim 7.

Col. 14, lines 20-26 in Picazo teach that the bridge process will realize that the machine having that destination address has been physically relocated to a different network segment, and will correct the bridge database entry for that destination address.

35 U.S.C. 102(b) rejection of claim 8.

Figure 9 in Picazo teach various memory buffers for partially storing packets.

35 U.S.C. 102(b) rejection of claims 9-13.

Figure 9 in Picazo teach that the first memory circuitry and the second memory circuitry comprise different portions of a single memory internal to the processor.

35 U.S.C. 102(b) rejection of claim 14.

Col. 24, lines 5-10 in Picazo teach that the use of forwarding vectors to flag bad packets that need to be dropped.

35 U.S.C. 102(b) rejection of claim 16.

See Figure 1 in Picazo.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Picazo, Jr.; Jose J. et al. (US 5720032 A, hereafter referred to as Picazo).

35 U.S.C. 103(a) rejection of claim 15.

Picazo substantially teaches the claimed invention described in claims 1-14 (as rejected above). In addition, Picazo teaches various host processors coupled to the hub/bridge processor of Figure 2 in Picazo (see Figure 1 in Picazo).

However Picazo does not explicitly teach the specific use of a host device to control the hub/bridge processor of Figure 2 in Picazo.

The Examiner asserts that it would be obvious an obvious engineering design choice to create an embodiment of the Picazo patent using a host device to control the hub/bridge processor of Figure 2 in Picazo based on available resources and resource requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Picazo by including use of a host device to control the hub/bridge processor of Figure 2 in Picazo. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a host device to control the hub/bridge processor of Figure 2 in Picazo would have provided the opportunity to implement an alternative embodiment of the Picazo patent based on available resources and resource requirements.

Conclusion

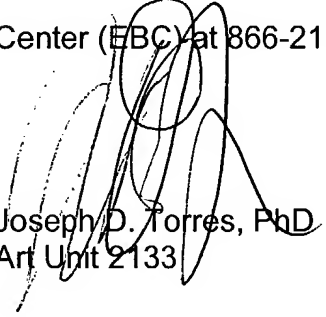
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishimura; Kazuto et al. (US 6754200 B1) teaches a rate control system of a TCP layer in communications conducted between two terminals which are connected via a wireless link. Balachandran; Kumar et al. (US 6115394 A) teaches communications networks which utilize packet communication protocols such as the Ethernet protocol.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2133

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133